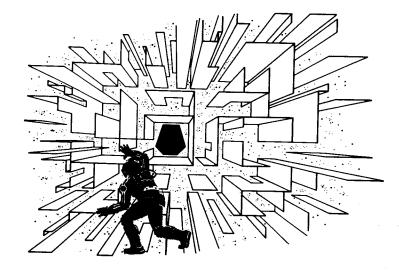
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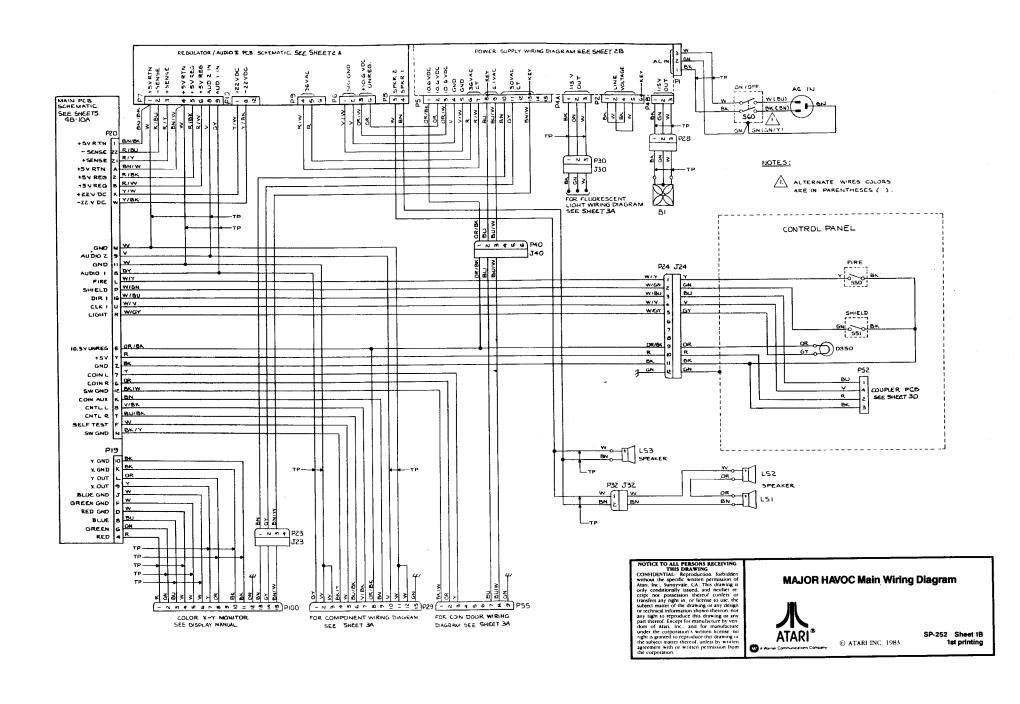


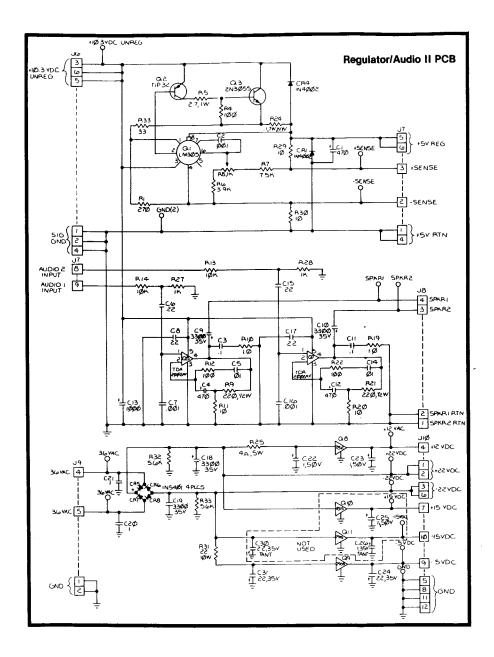
## **Schematic Package Supplement to**



**Operators Manual** 







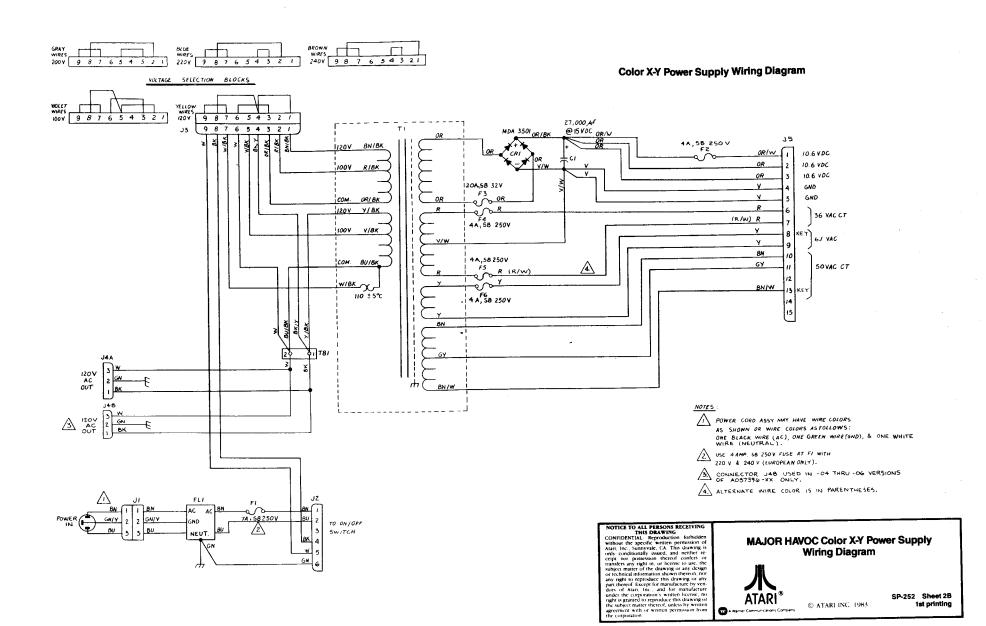
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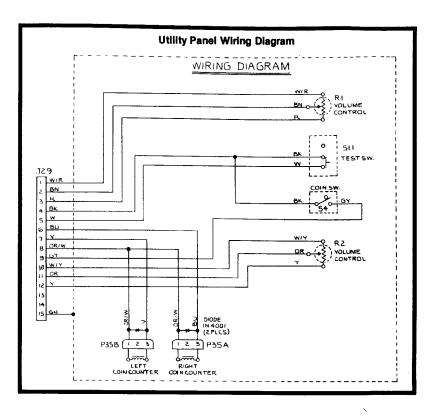
## **MAJOR HAVOC Regulator/Audio II PCB** Schematic Diagram

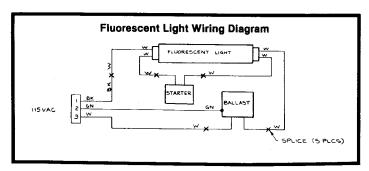


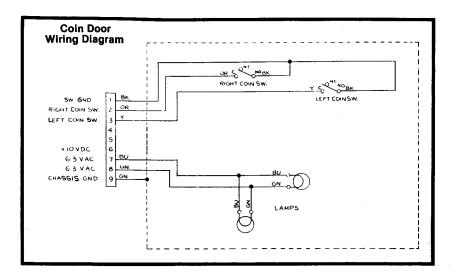
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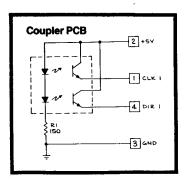
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## **MAJOR HAVOC Game Interfaces**



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# Major Havoc Memory Map Alpha (α) Microprocessor

IEXA-		ADDRESS BUS SIGNAL LINES R																READ/	DATA BUS SIGNAL LINES							ES		
DECIMAL ADDRESS	A15	A14	A13	A12	A1	DD	RES	<u>SS B</u>	AS	SIGI A7	<u> 141</u>	A5	A4	A3	A2	A1	AO		D7	D6	D5	D4	D3	D2	D	1 I	20	FUNCTION
							_								_			R/W	D	D	D	D	D	D	1	)	D	PROGRAM RAM (1/2K)
0000-01FF	0	0	0	0	0	(	-	0	A	A	A	A	A	A	A		A	R/W	D	D	D	Ď	Ď	D		)	D	PAGED PROGRAM RAM (3K)
0200-07FF	0	0	0	0	0	1		A	A	A	٨	A	A	A	A	A		R/W	D	D	D	D	D				D	PROGRAM RAM (1/2K)
0800-09FF	0	0	0	0	1	(	)	0	A	٨	٨	A	A	A	A	A	A	N.*		D	_	_	_	~	_			111001111111111111111111111111111111111
1000	0	0	0	1	0	(	0	0										R	D	D	D	D	D	D	I	)	D	GAMMA COMM, READ PORT
1200	0	0	0	1	0		0	1										R	D									RIGHT COIN SW. (PLAYER 1=0)
1200	ő	0	ō	1	0		-	1										R	1	D								LEFT COIN SW. (PLAYER 1=0)
1200	lő	0	ŏ	î	0		~	i										R			D							AUX. COIN SW. (PLAYER 1=0)
1200	ŏ	0	0	î	0		-	î										R	D									SELF-TEST (PLAYER 1=1)
1200	١٥	0	n	1	0		~	î										R	1	D								CABINET SW. (PLAYER 1=1)
1200	0	0	0	1	0		•	1										R			D							AUX. COIN SW. (PLAYER 1=1)
1200	0	0	0	•	0		_	1										R	1				D					GAMMA RCVD FLAG
	1 0	0	0	1	0		~	1										R	l					D				GAMMA XMTD FLAG
1200		0	0	1	0		-	1										R	1						1	D		2.4KHz
1200	0		-	1	0		-	1										R	i								D	VEC. GEN. HALT FLAG
1200	°	0	0	1	U		U	1										1 "	1									
1400-141F	0	0	0	1	C	)	1	0					A	A	A	A		w					D	) D	) [	D	D	COLORAM
1600	١٠	0	0	1	0	,	1	1	0	0	0.							w	D									INVERT Y
1600	ŏ	0	-	i	Č		i	1	0	0	0							w	1	D								INVERT X
1600	ا o	ō	-	ī	Č		1	1	ō	o	0							w	ł		D							PLAYER 1
1600	l ŏ	0		1			î	i	ŏ	ō	ō							w	١.				Đ	)				GAMMA RESET
1600	١٥	0	_	1			i	i	ō	o	ō							l w									D	ROLLER CONTROL LIGHT
1000	ľ	٠	٠	•	•		•	•	•	•	Ť							1										
1640	0	0	0	1	(	)	1	1	0	0	1							w	1.									VEC. GEN. GO
1680	0	0	0	1	(	)	1	1	0	1	0							w	1								-	WATCHDOG CLEAR
16C0	lo	O		1			1	1	0	1	1							w	1									VEC. GEN. RESET
		_		-						_	^							w	1									IRO ACKNOWLEDGE
1700	0	0	-				1		1	0	0							w	1									PROGRAM ROM MMU
1740	0	0	-			)	1	1	1	0	1							w										PROGRAM RAM SELECT
1780	0	(				0	1	1	1	1	0							w	1									GAMMA COMM. WRITE PORT
17C0	0	C	0	1	. 1	0	1	1	1	1	1							1 "	l									
2000-3FFF	0	(	) 1	A	١.	A	A	A	A	A	A	A	A	. A	. 4	-		R	P	_	-					D	D	PAGED PROG. ROM (32K)
4000-4FFF	0	- 1	0	0	) .	A	A	A	A	A	Α	A	A	. А	. /			R/W	D		_		_			D	D	VEC. GEN. RAM (4K)
5000-5FFF	0	- 1		1	١.	A	A	A	Α	A	A	A	A	. A		. /	A A	R	D						_	D	D	VEC. GEN. ROM (4K)
6000-7FFF	Ιŏ	1	1	1	١.	٨	A	A	A	A	A	A	A		. /	. /	A A	R	D		_				D	D	D	PAGED VEC. GEN. ROM (32K)
8000-FFFF	l i	1		. Ā		A	Α	A	A	A	A	A	A				A A	R	D	. [	) [	) [	) 1	D I	D	D	D	PROGRAM ROM (32K)

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**MAJOR HAVOC Memory Map** Alpha ( $\alpha$ ) Microprocessor



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# Major Havoc Memory Map Gamma $(\gamma)$ Microprocessor

HEXA- DECIMAL ADDRESS	A1:	5 A	14	<b>A13</b>	A12	AI AII	DDI A1	RES	S B	US A8	SIG A7	NAL A6	LIN A5	ES A4	<b>A3</b>	A2	A1	ΑO	READ/ WRITE				JS SI D4					FUNCTION
0000-07FF 2000-203F	0		0	0 1	0	0	A	_	A	A	٨	A	A A	A A	A A	A A	A A	A A	R/W R/W	D D	D D	D D	D D	D D	D D	D D	D D	PROGRAM RAM (2K) QUAD. CUSTOM I/O
2800 2800 2800 2800 2800 2800 2800	0 0 0 0 0		0 0 0 0 0	1 1 1 1 1	0 0 0 0 0	1 1 1 1 1													R R R R R	D	Ď	đ	D			D	D	FIRE 1 SWITCH SHIELD 1 SWITCH FIRE 2 SWITCH SHIELD 2 SWITCH ALPHA RCVD FLAG ALPHA XMTD FLAG
3000 3800-3803	0		0	1	1	0											A	٨	R R	D D	D D	D D	D D	D	D D		D D	ALPHA COMM. READ PORT ROLLER CONTROL INPUT
4000 4800 4800 5000 6000–61FF 8000–BFFF	0 0 0 0 0		1 1 1 1	0 0 0 0 1 A	0 0 0 1	0 1 1 0	A		A	A A	A A	A A	A A	A A	A A	A A	A A	 A A	W W W R/W	D D	D D	D D	D D	D D	D D	D D D	D D D	IRQ ACKNOWLEDGE LEFT COIN COUNTER RIGHT COIN COUNTER ALPHA COMM. WRITE PORT EEROM PROGRAM ROM

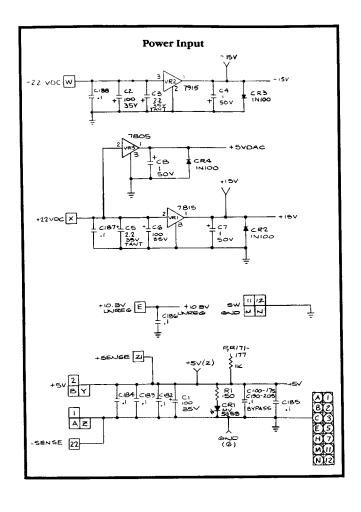
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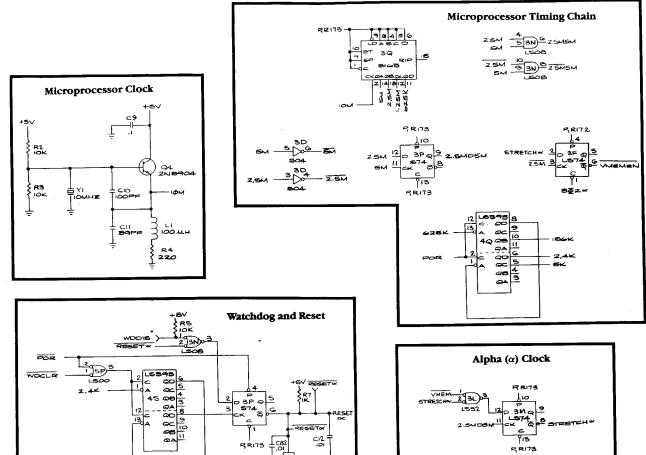
**MAJOR HAVOC Memory Map** Gamma ( $\gamma$ ) Microprocessor



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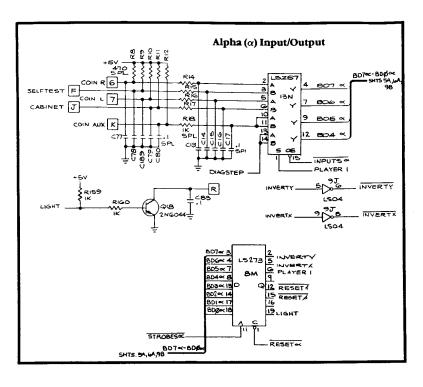
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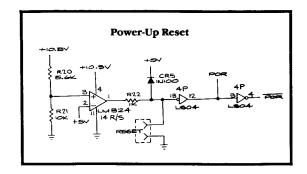


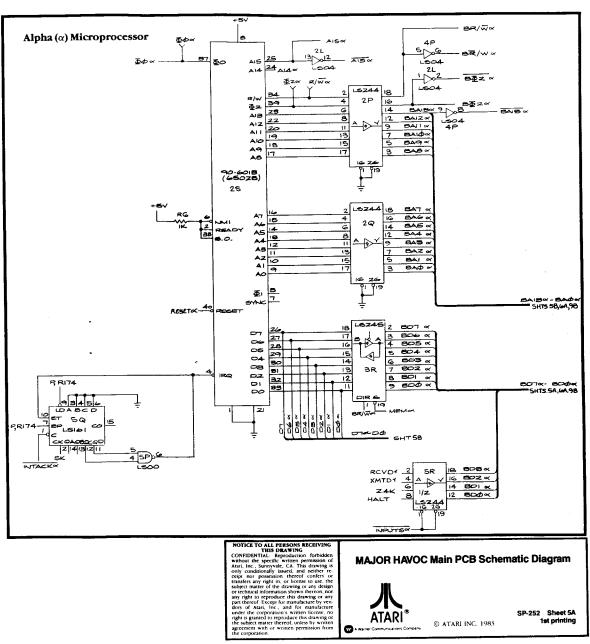
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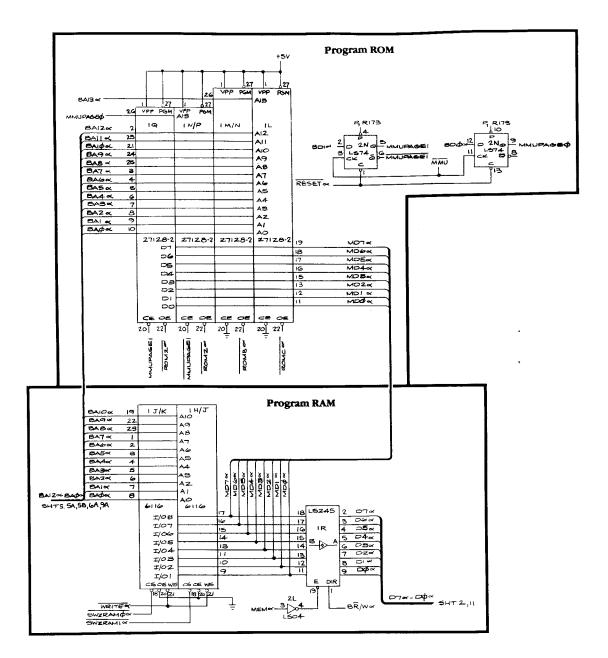


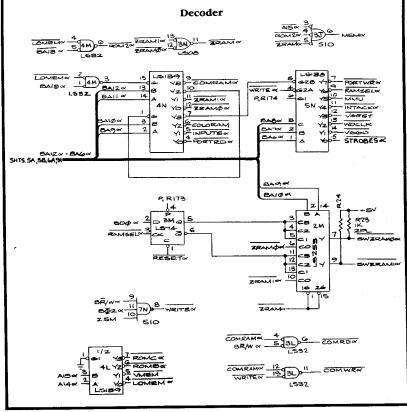


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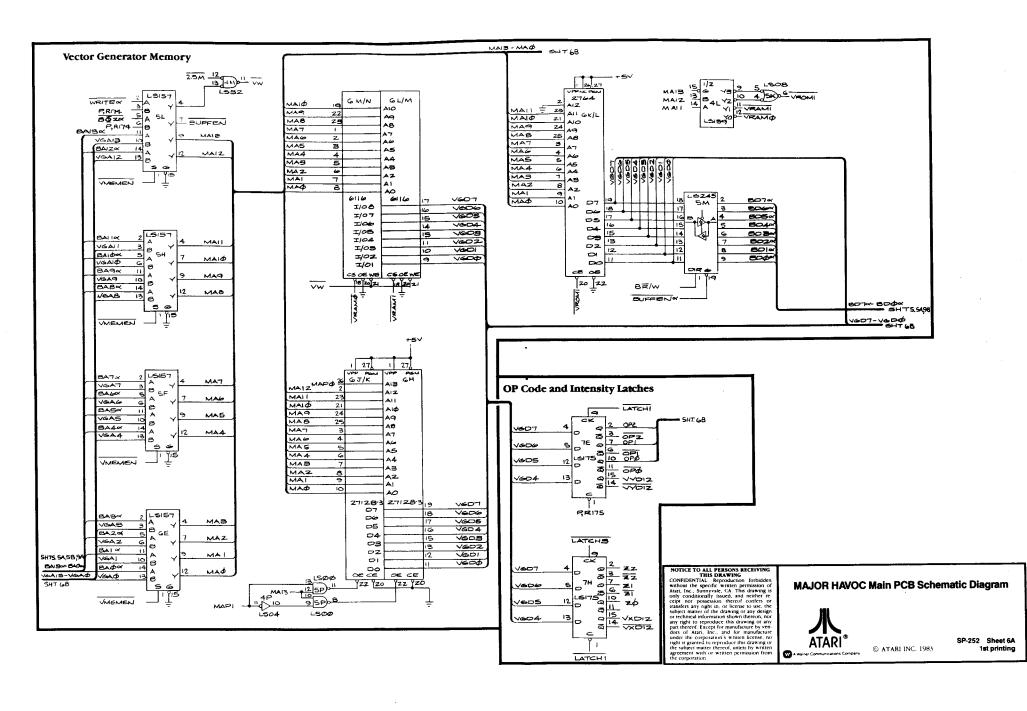
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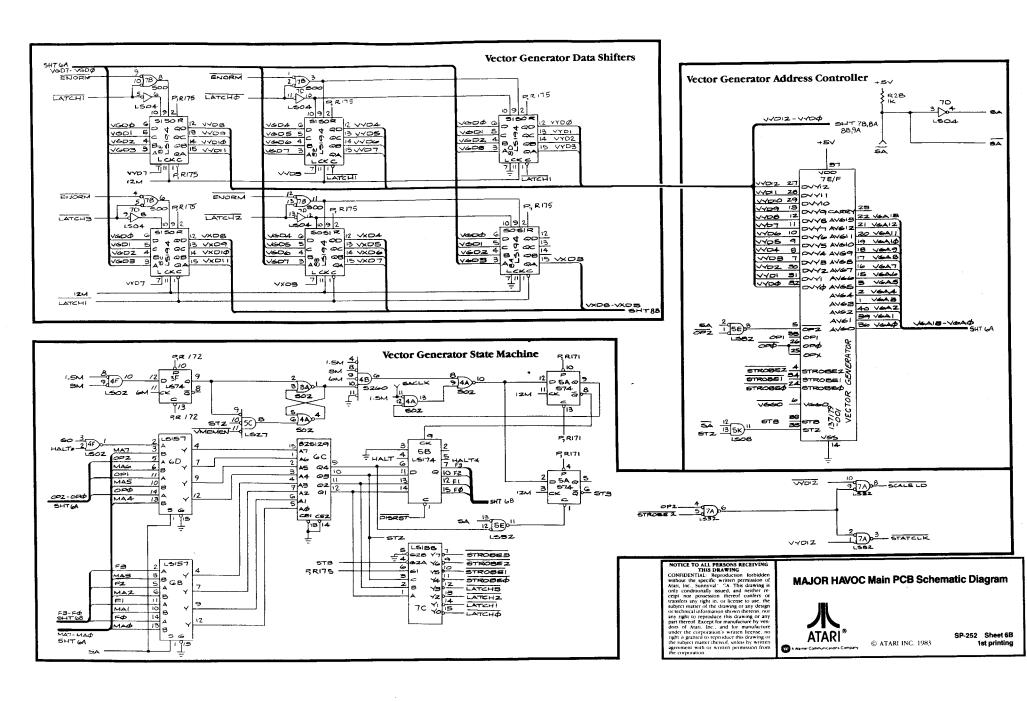
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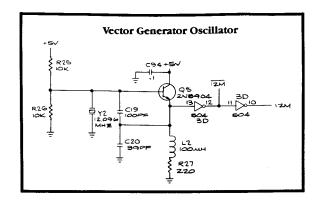


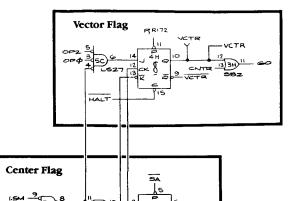
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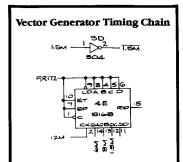


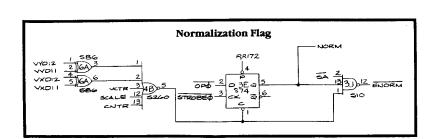






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# Halt Flag RESET DISRST

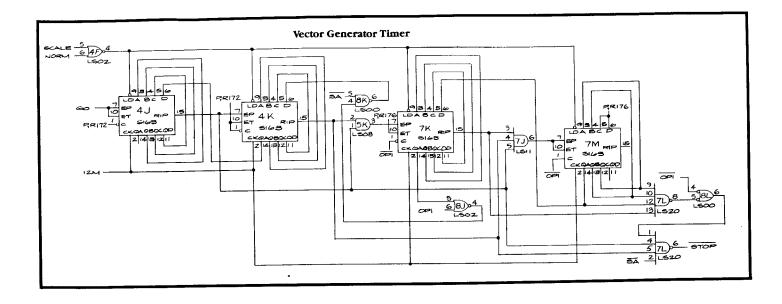
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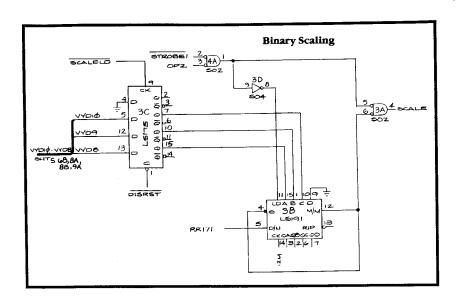
## MAJOR HAVOC Main PCB Schematic Diagram



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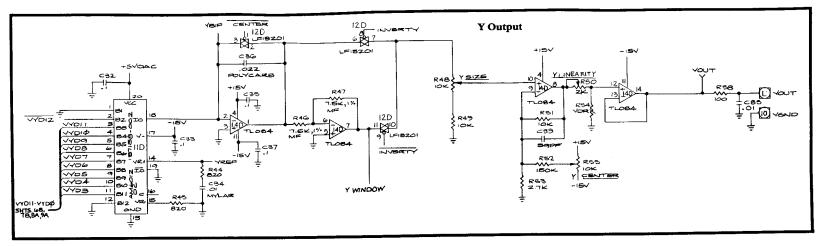
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## MAJOR HAVOC Main PCB Schematic Diagram



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## X and Y Video Adjustments

Perform the following procedure to adjust the display size, centering, and linearity:

1. Set the game to the Self-Test Mode and select the Crosshatch Pattern Display as described in Chapter 2 of the game manual.

SHT 68 VXDI I-VXD3 VXD3

5)9A)

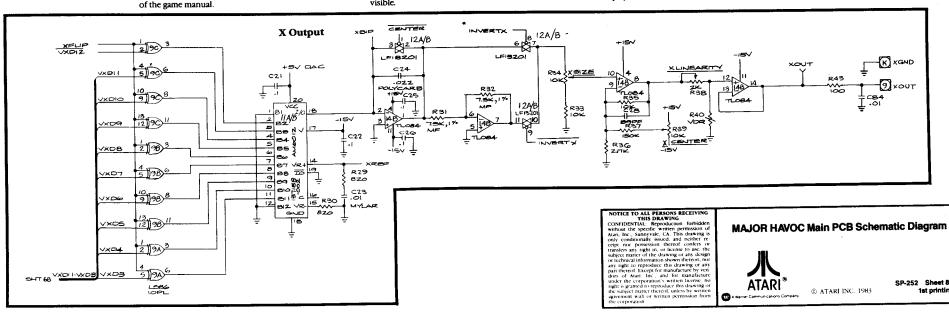
- 2. Adjust XCENTER (R39) and YCENTER (R55) so that the crosshatch pattern is centered on the screen.
- 3. Adjust XSIZE (R34) and YSIZE (R48) so that all four corners of the red outline are off the screen and all four corners of the white outline are completely visible.
- Adjust XLINEARITY (R38) and YLINEARITY (R50) so that the diagonal lines are straight and the diamondshaped squares are symmetrical. Since the linearity potentiometers change the size of the display, it may be necessary to repeat step 3 to obtain the correct display.

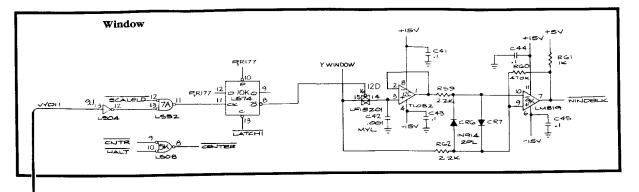
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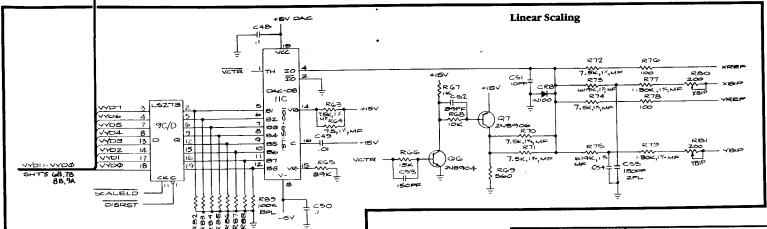




## **Bipolar Offset Adjustments**

Perform the following procedure to adjust the bipolar offset current:

- 1. Set the game to the Self-Test Mode and select the Bipolar Offset Test Display as described in Chapter 2 of the game manual.
- 2. Adjust XBIP (R80) and YBIP (R81) so that the lines in the center of the screen cleanly overlap to form a single orange square. The upper right-hand corner of the orange square is the critical adjustment point.



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**MAJOR HAVOC Main PCB Schematic Diagram** 



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